developing the hardware model and the software concurrently; and

communicating command and control information directly between the CPU server and the CPU bus functional model over the network, and communicating command information directly between the CPU bus functional model and the CPU server over the network to co-simulate the hardware model and the software while the hardware model and the software are being developed.

2. (Amended) The method of claim 1, wherein the hardware model is developed on a workstation.

8. (Amended) A method of co-simulating a hardware model and a software in ASIC development, the hardware model comprising a CPU bus functional model, the software being coupled to a CPU server and communicating with the hardware model via a network coupled to the bus functional model and the CPU server, the method comprising:

requesting an access to the hardware model from the software via the network;

invoking a function call by the CPU server;

sending an access request from the bus functional model to the CPU server via the network;

routing the access request to the hardware model;

developing the hardware model and the software concurrently; and

co-simulating the hardware model and the software while the hardware model and the software are being developed.

12. (Amended) An apparatus for hardware model and software co-simulation in ASIC development, comprising:

a hardware model, the hardware model representing a hardware board circuit to be co-simulated/tested, the hardware model being developed on a workstation and including a CPU bus functional model;

a software, the software providing command and control access of the hardware model, the software being developed/debugged on a target board concurrently with a design of the hardware model, the target board including a CPU server in communication with the software; and

a network coupled between the CPU bus functional model and the CPU server to communicate a command from the software to the hardware model and to route contents of the command between the hardware model and the software, thereby providing co-simulation of the hardware model and software.

14. (Amended) The apparatus of claim 12, wherein the software is loaded on the CPU server.